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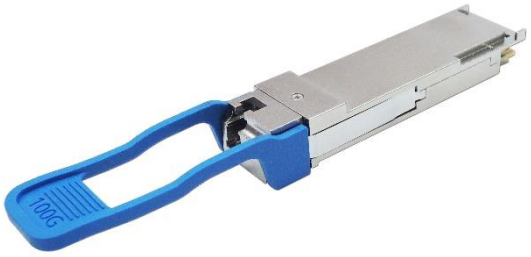
Rev.00C3.30_20240110

100G Single Lambda ER1-30-BiDi Transceiver
Hot Pluggable, Bidi LC, Tx1304nm EML / Rx1309nm, SMF 30KM, DDM

Part Number: FQ2S-K8-L04-30D



Overview

FQ2S-K8-L04-30D is a QSFP28 Single Lambda BIDI transceiver for 100GbE applications especially in Datacom, Data Center & Storage networks applications. It works based on the 100G Lambda MSA 100G-ER1-30 Standard with the typical center wavelength 1304nm. The transceiver incorporates one channel optical signal of 100Gbps(PAM4) from four channels electrical signal of 25Gbps(NRZ) and vice versa up to SMF 30km optical links.

Applications

- 100GBASE Ethernet
- Data Centers Switch Interconnect
- Server and Storage Area Network Interconnect

Features

- Compliant with SFF-8665 QSFP28 MSA
- Compliant with IEEE 802.3bm CAUI-4 Interface
- Compatible with 100GBASE-ER1-30
- Signal Conversion between 53.125GBd PAM4 optical signal and 25.78125Gbps NRZ electrical signal with DSP Gear Box
- Built in Tx CDR and Rx CDR
- Inbuild KP4 FEC
- Hot Pluggable QSFP28 footprint
- LWDM 1304nm EML transmitter
- APD receiver
- Simplex LC connector
- 2-wire interface for management and diagnostic monitor compliant with SFF-8636
- Single 3.3V power supply
- Operating Temperature 0~70°C
- Link distance 30km over SM fiber with FEC
- Maximum Power consumption 4.5W
- RoHS compliant

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Laser Safety

- This is a Class 1 Laser Product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
- Caution: Use of control or adjustments or performance of procedure other than those specified herein may result in hazardous radiation exposure.

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T_{ST}	-40	+85	°C
Storage Relative Humidity	RH	5	95	%
Supply Voltage	V_{CC3}	-0.5	+3.6	V

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T_{OP}	0	-	+70	°C
Supply Voltage	V_{CC}	+3.13	+3.3	+3.47	V
Supply Current	I_{CC}			1360	mA
Electrical Data Rate, per Lane (NRZ)	DR_{ELE}		25.78125		Gb/s
Optical Data Rate (PAM4)	DR_{OPT}		53.125		GBd
Data Rate Accuracy	ΔDR	-100		+100	ppm
Pre-FEC Bit Error Rate	BER_{PRE}			$2.4x10^{-4}$	
Post-FEC Bit Error Rate	BER_{POST}			$1x10^{-12}$	
Power Consumption	P			4.5	W
Transceiver Power-on Initialization Time				2000	ms
Control Input Voltage High	V_{IH}	2.0		Vcc+0.3	V
Control Input Voltage Low	V_{IL}	-0.3		0.8	V
Fiber Link Distance (G.652 SMF)	D			30	km

Transmitter Electro-optical Characteristics

V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters		Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate		DR		103.125	106.25	Gb/s	
Optical Center Wavelength		λc	1304.06	1304.58	1305.1	nm	
Average Launch Power		P_{AVG}	0		+5.6	dBm	
Optical Modulation Amplitude (OMA)	TDECQ < 1.4dB	P_{OMA}	+3.0		+6.4	dBm	
	TDECQ > 1.4dB.		1.6+ TDECQ		+6.4	dBm	
Transmitter and Dispersion Eye Closure		TDECQ			3.9	dB	
Spectral Width (-20dB)		Δλ			1	nm	
Side Mode Suppression Ratio		SMSR	30			dB	
Optical Extinction Ratio		ER	5			dB	
Relative Intensity Noise		RIN			-136	dB/Hz	
Average Launch Power OFF		P_{OFF}			-30	dBm	
Optical Return Loss Tolerance		ORLT			15.6	dB	
Transmitter Reflectance		R_{TX}			-26	dB	
Input Differential Impedance		Z_{IN}	90	100	110	Ω	
Differential Data Input Voltage		V_{IN-PP}	900			mVpp	
Common Mode Voltage (Vcm)		TP1	-350		2850	mV	

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Receiver Electro-optical Characteristics

V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters		Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate		DR		103.125	106.25	Gb/s	
Optical Center Wavelength		λc	1308.61	1309.14	1309.66	nm	
Damage Threshold		D_{TH}	-2.4			dBm	1
Average Receive Power		P_{RX-AVG}	-14.7		-3.4	dBm	
Receiver Power (OMA)		P_{RX-OMA}			-2.6	dBm	
Receiver Sensitivity (OMA)	TDECQ < 1.4dB	SEN_{OMA}			-12.5	dBm	2
	TDECQ > 1.4dB.				TECQ-13.9		
Stressed Receiver Sensitivity (OMA)		SRS_{OMA}			-10	dBm	
Receiver Reflectance		R_{RX}			-26	dB	
LOS De-Assert		LOS_D			-16	dBm	
LOS Assert		LOS_A	-26		-18	dBm	
LOS Hysteresis		LOS_{HY}	0.5			dB	
Output Differential Impedance		Z_{OUT}	90	100	110	Ω	
Differential Data Output Voltage		V_{OUT-PP}			900	mVpp	
Common Mode Voltage (Vcm)		TP4	-350		2850	mV	

Note1: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

Note2: Sensitivity is specified at $2.4x10^{-4}$ BER with PRBS31Q.

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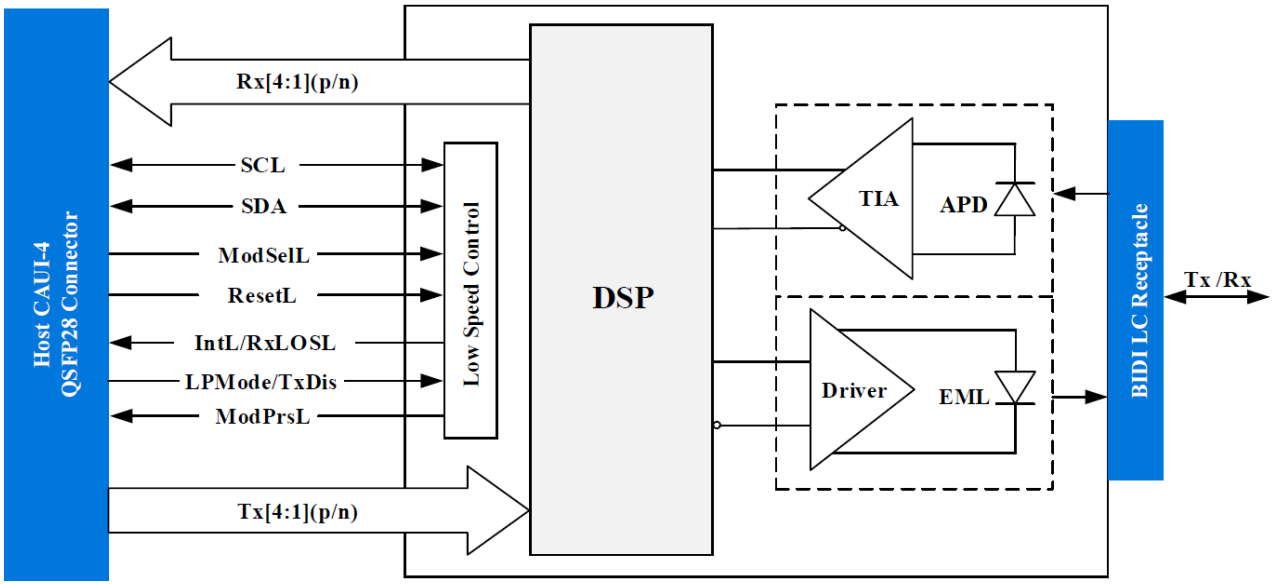
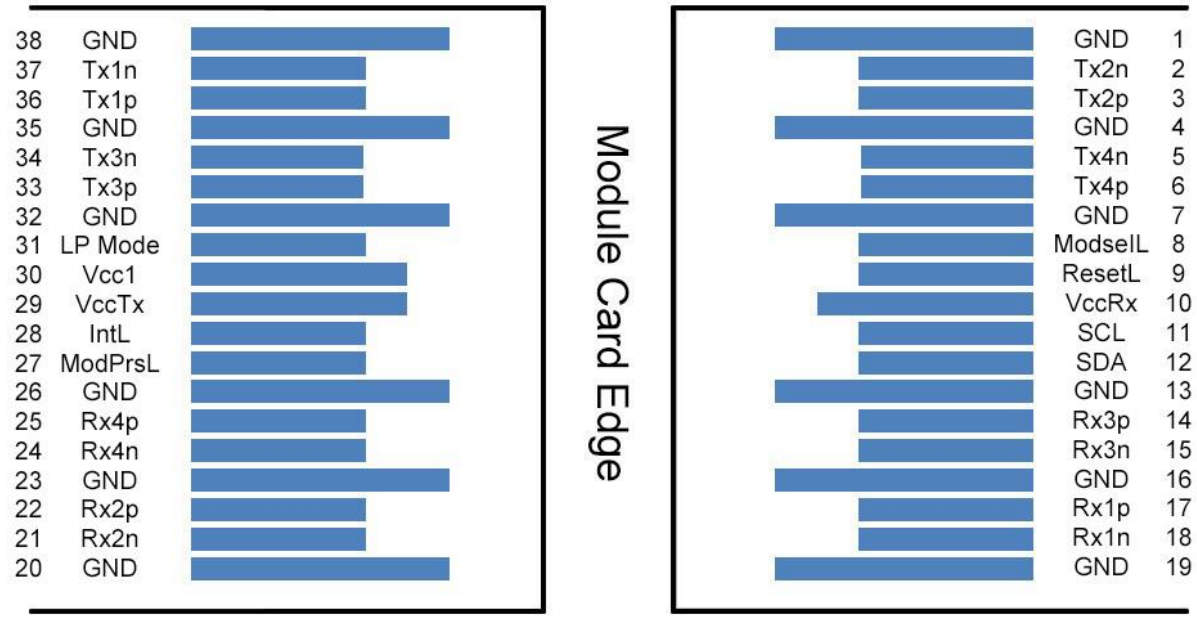
Transceiver Block Diagram



Pin Assignment



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin Description

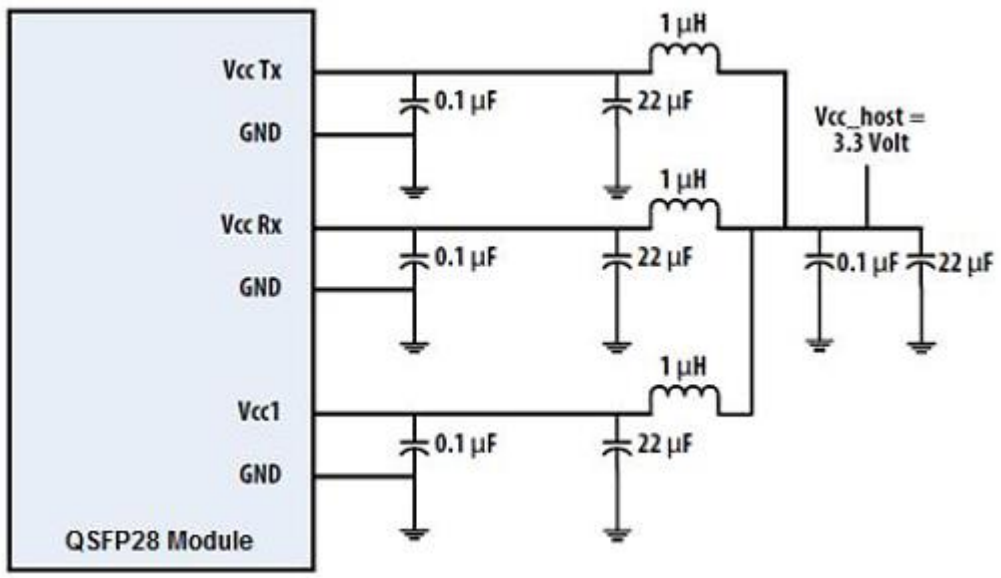
Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMode	Low Power Mode
32		GND	Module Ground

33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Module Ground

Note1: GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

Note2: VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Recommended Power Supply Filter



Digital Diagnostic Functions

As defined by the QSFP28 MSA, Ficer's QSFP28 transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP28 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP28 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP28 MSA Specification.

Digital Diagnostic Memory Map

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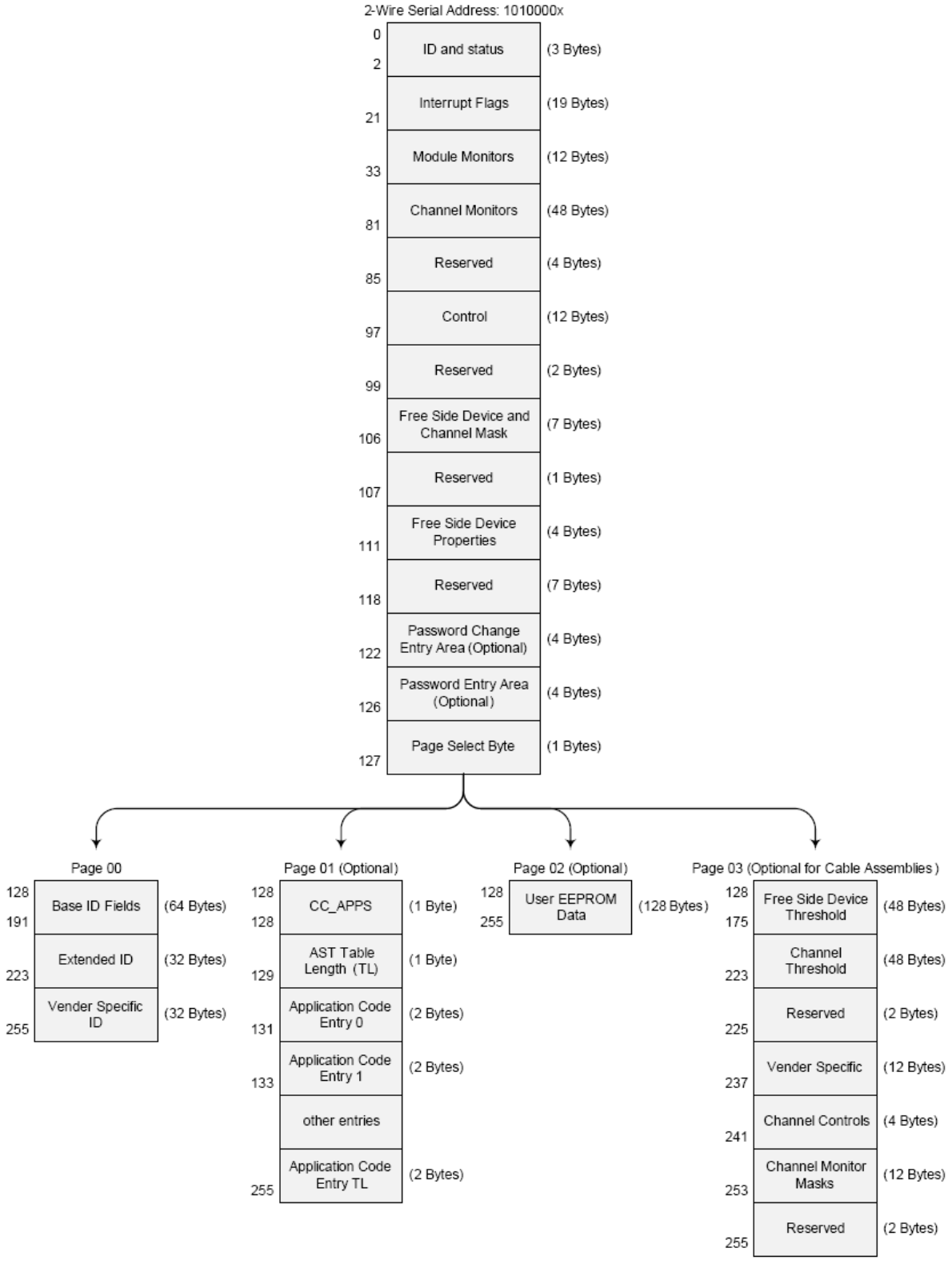
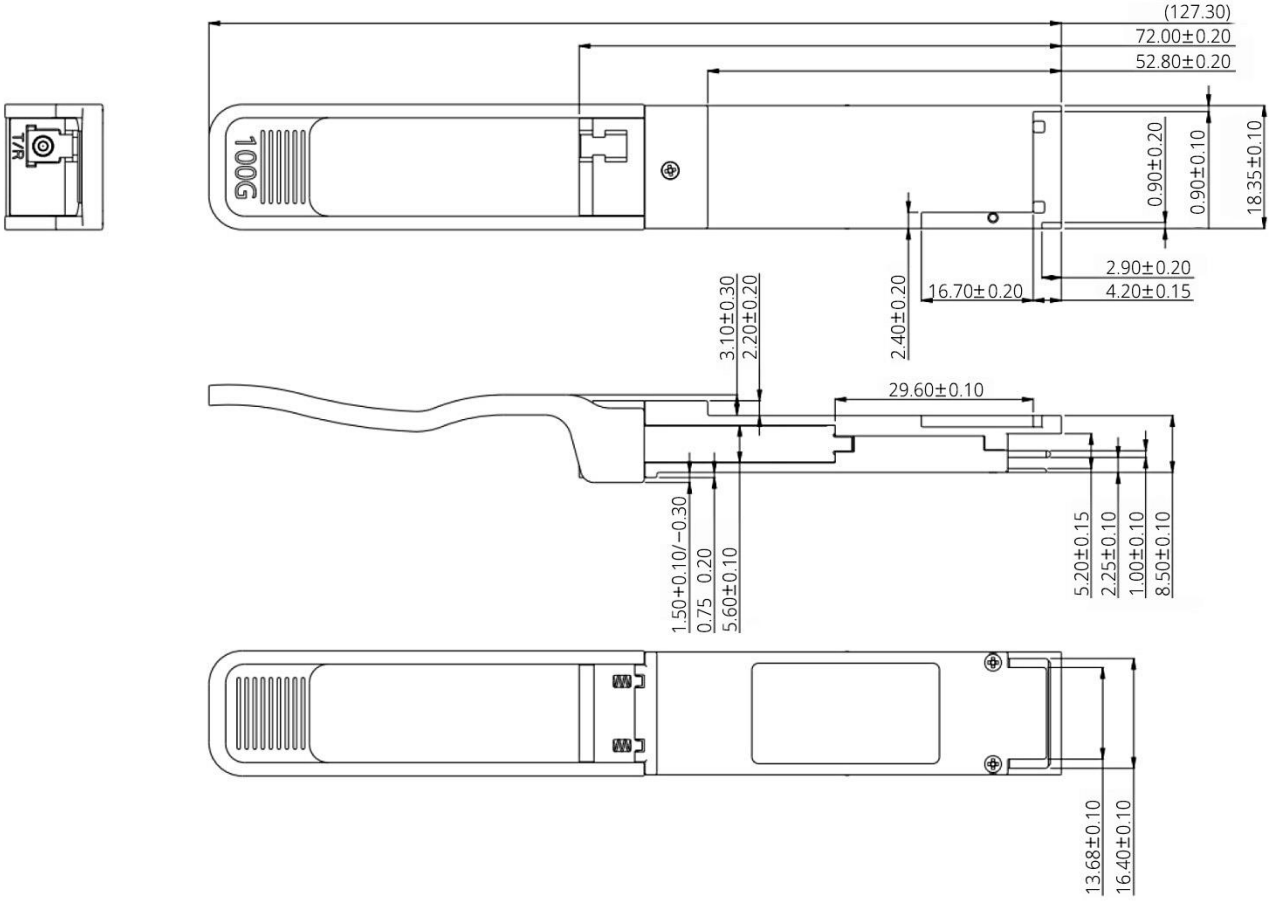

2-Wire Serial Address: 1010000x
0
ID and status (3 Bytes)
2
Interrupt Flags (19 Bytes)
21
Module Monitors (12 Bytes)
33
Channel Monitors (48 Bytes)
81
Reserved (4 Bytes)
85
Control (12 Bytes)
97
Reserved (2 Bytes)
99
Free Side Device and Channel Mask (7 Bytes)
106
Reserved (1 Bytes)
107
Free Side Device Properties (4 Bytes)
111
Reserved (7 Bytes)
118
Password Change Entry Area (Optional) (4 Bytes)
122
Password Entry Area (Optional) (4 Bytes)
126
Page Select Byte (1 Bytes)
127
Page 00
128
Base ID Fields (64 Bytes)
191
Extended ID (32 Bytes)
223
Vender Specific ID (32 Bytes)
255
Page 01 (Optional)
128
CC_APPS (1 Byte)
128
AST Table Length (TL) (1 Byte)
129
Application Code Entry 0 (2 Bytes)
131
Application Code Entry 1 (2 Bytes)
133
other entries
Application Code Entry TL (2 Bytes)
255
Page 02 (Optional)
128
User EEPROM Data (128 Bytes)
255
Page 03 (Optional for Cable Assemblies)
128
Free Side Device Threshold (48 Bytes)
175
Channel Threshold (48 Bytes)
223
Reserved (2 Bytes)
225
Vender Specific (12 Bytes)
237
Channel Controls (4 Bytes)
241
Channel Monitor Masks (12 Bytes)
253
Reserved (2 Bytes)
255

Mechanical Dimensions



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

Ordering Information

Part No.	Tx	Rx	Link	DDM	Temp.
FQ2S-K8- L04-30D (Blue Pull Tab)	1304nm	1309nm	SMF 30km (with FEC)	Yes	0~70°C

Note1: Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics.

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